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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,929	02/25/2004	Junichi Naka	2004_0299A	9592

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WENDEROTH, LIND & PONACK, L.L.P.
2033 K STREET N. W.
SUITE 800
WASHINGTON, DC 20006-1021

EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/784,929	NAKA ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *5-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of group I, claims 1-4 in the reply filed on 05/17/05 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Tomishima et al. (US 2003/0007296).

As to claim 1, Tomishima et al.'s figure 16 shows a standard voltage generation circuit comprising: a standard voltage generation circuit body (the most left QD1) for generating a standard voltage; a standard voltage stabilization capacitor (692) for stabilizing the standard voltage; and a standard voltage rapid stabilizer (the most right QD1) for rapidly stabilizing the standard voltage.

As to claim 2, figure 16 shows that the standard voltage rapid stabilizer comprises a rapid charging/discharging current source which performs rapid charging or rapid discharging to/from the standard voltage stabilization capacitor.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ooishi (USP 6191994) in view of Tomisima et al. (US 2003/0007296).

As to claim 1, Ooishi's figure 1 shows a standard voltage generation circuit comprising: a standard voltage generation circuit body (10, 12) for generating a standard voltage; and a standard voltage rapid stabilizer (17) for rapidly stabilizing the standard voltage. Thus, figure 1 shows all limitations of the claim except for "a standard voltage stabilization capacitor for stabilizing the standard voltage". However, Tomishima et al.'s figure 16 shows a voltage generation circuit having stabilization capacitor for stabilizing the generated voltage. Therefore, it would have been obvious to one having ordinary skill in the art to add a stabilizing capacitor to Ooishi's figure 1 for the purpose of further stabilizing the voltage at node N6.

As to claim 2, the modified Ooishi et al.'s figure 1 shows that the standard voltage rapid stabilizer comprises a rapid charging/discharging current source which performs rapid charging or rapid discharging to/from the standard voltage stabilization capacitor.

As to claim 3, the modified Ooishi et al.'s figure 1 shows that the rapid charging/discharging current source comprises: a bias current source (20) for outputting a predetermined current; and a current mirror circuit (17, 18) including a first conductivity type first transistor (18) having a source connected to a first voltage, a drain connected to the bias current source, and a gate and the drain being short-circuited, and a first conductivity type second transistor (17) having a source connected to the first voltage, a drain connected to the

standard voltage stabilization capacitor, and a gate connected to the gate of the first conductivity type first transistor.

As to claim 4, the modified figure 1 shows that the rapid charging/discharging current source comprises: a bias current source (20) for outputting a predetermined current; and a current mirror circuit (17, 18) including a second conductivity type first transistor (18) having a source connected to a second voltage, a drain connected to the bias current source, and a gate and the drain being short-circuited, and a second conductivity type second transistor (17) having a source connected to the second voltage, a drain connected to the standard voltage stabilization capacitor, and a gate connected to the gate of the second conductivity type first transistor.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

June 13, 2005